PHASE CHARACTERISTICS OF I-BAND PULSED GATE GaAs FET POWER AMPLIFIERS*

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ABSTRACT

The measured phase sensitivities and transients of FET power amplifiers having pulsed gate voltages are very low and are suitable for phased array applications. Gate pulsing requires that the FETs have good rf performance and a drain-to-gate breakdown voltage large enough to support the sum of the gate voltage, drain voltage, and maximum rf voltage swing.

Introduction

In pulsed phase array applications, such as airborne radar, both amplitude and phase characteristics of microwave amplifiers must be precisely known under pulsed conditions. Moreover, the differential phase shift obtained between amplifiers must be held within controlled limits to ensure minimum error in a phased array. Power FET amplifiers, which have recently become available for application at I-band frequencies (8-10 GHz), and which have significant advantages in terms of potential reliability, low voltage operation, low noise, and size and weight, have not previously been considered for these applications because suitable techniques for pulsing such amplifiers had not been developed. Furthermore, the intrapulse and interpulse phase properties of such amplifiers have not been studied.

This paper will present the phase sensitivities of several amplifier stages using different FET geometries as a function of gate voltage, drain voltage, VSWR, temperature, and rf input level under both cw and pulse conditions. The amplitude and phase characteristics of a complete five-stage amplifier including special pulse modulation biasing circuitry will be described. It will thus be shown that the microwave power FET amplifier is suitable for pulsed phased array systems.

Pulsing Techniques of FET Amplifiers

To maintain high efficiency during pulsed rf conditions, the dc power supplied to the amplifier must be pulsed on only when rf signal is present. This is achieved in a FET amplifier by pulsing the drain current.

The FET drain current can be controlled by changes in either the gate or drain voltage. In gate pulsing, the gate voltage is switched between a low negative voltage which results in efficient rf power amplification and a higher negative voltage near the pinchoff voltage of the FET which effectively turns off the drain current. In drain pulsing, the drain voltage is switched between the level needed for efficient power amplification and zero volts. Drain pulse bias modulation circuitry must handle large currents and because losses of drain modulation degrade overall amplifier efficiency, amplifiers were fabricated using gate pulsing. It was found however that gate pulsing requires that the FET meet dc voltage breakdown limits and rf performance levels which are difficult to satisfy simultaneously. The drain-to-gate breakdown voltage must be large enough to support the sum of the drain voltage, the gate voltage, and the peak rf voltage; this sum can be as high as 15 to 20 volts. The tradeoffs between gate and drain pulsing must be investigated further.

Phase Sensitivities

It is necessary to determine the variation in phase shift of pulsed FET amplifiers as a function of gate voltage, drain voltage, temperature, load variations, and drive levels. Under cw conditions, these can readily be determined with a special automatic network analyzer system which incorporates a system of step attenuators under computer control to permit vector measurements under varying high power levels. To permit similar measurements during both pulsed and cw conditions, a special phase measurement bridge was set up using standard waveguide components as shown in Fig. 1. The output of this bridge is provided by a

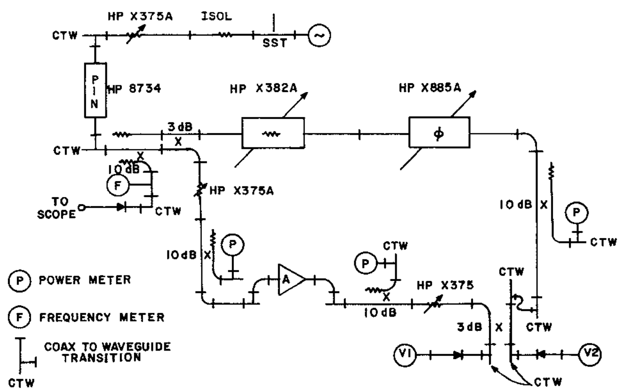

Figure 1. Pulsed phase measurement bridge.

pair of hybrid-coupled detectors driving a differential amplifier oscilloscope plug-in. This arrangement provides a well-defined high sensitivity null which does not require equal power levels in each arm of the bridge. Nulls are achieved and vertical sensitivities in degrees/division are determined by adjustment of the calibrated waveguide phase shifter.

The phase sensitivities of single stage amplifiers using different type FETs have been measured with the phase bridge. The pertinent characteristics are summarized in Table 1. It is seen that the phase sensitivity to the gate potential is greatest for small signal devices while the sensitivity to drain voltages is greatest for the large signal devices. These data show that the greatest amount of voltage regulation is needed at the gate.

Transient data can readily be determined even when

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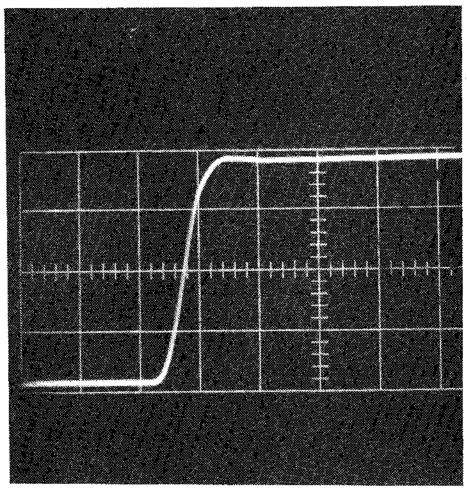
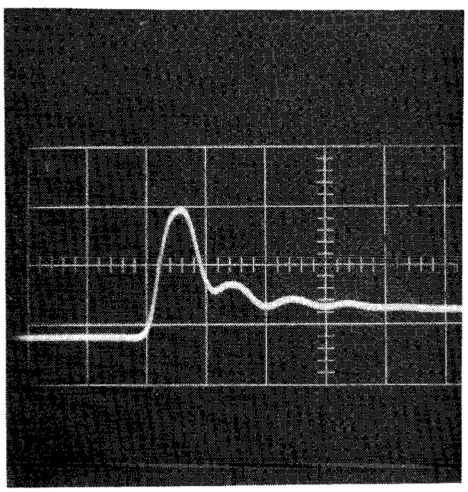
TABLE 1. FET Amplifier Stage Phase Sensitivities

	Number of Parallel Gates		
	2	4	16
Gate Width (μm)	300	600	2400
$\Delta\phi/\Delta V_{drain}$	$\pm$ 1°/V	- 2°/V	- 3°/V
$\Delta\phi/\Delta V_{gate}$	12°/V	8°/V	6°/V
$\Delta\phi/\Delta VSWR$		6°	
$\Delta\phi/\Delta T$		0.66°/°C	

both rf and gate voltages are pulsed. Typical turn-on responses are shown in Fig. 2. Figure 2a shows the amplitude response with the rf pulse and gate voltage turned on simultaneously. The amplitude reaches its final response within 40 nsec. This response is identical to that of the input rf pulse. The phase transient response is shown in Fig. 2b when the trailing edge of the pulse (not shown) is set to zero degrees. After an initial overshoot of 7° (caused by small length differences in the arms of the phase bridge) the phase shift 60 nsec after pulse turn-on is 1.5°.



(a) 40 ns/div.



(b) 40 ns/div.

Figure 2. Pulse responses of a 4-gate single cell amplifier: (a) amplitude response; (b) phase response.

Multi-Stage Amplifier Phase Responses

A five-stage FET amplifier including pulse modulators in the gate bias circuitry has been fabricated. This amplifier has an output of 500 mW with over 27 dB gain covering the 9-10 GHz band. A schematic representation of the overall FET amplifier bias and video pulse circuitry is shown in Fig. 3. Only the last two stages are pulsed; in the absence of rf drive, this reduces dissipation by 70%. These two stages are cut off with -4 V applied to the gates. The output stage is turned on with a -1.5 V gate bias while the preceding stage requires 0 V. These different voltages are generated by the pulse modulation circuitry.

To determine the amplifier suitability to phase array applications, extensive testing has been done under three different modes of operation, namely, cw, pulsed rf, and pulsed rf during pulsed gate bias. The cw performance of the amplifier at the center frequency of 9.5 GHz is summarized in Fig. 4. The FET amplifier shows virtually identical performance under pulsed rf conditions as shown in Fig. 5. These measurements are made with an rf pulse width of 100 μsec at a duty cycle of 50%. The AM/PM ranges from +3.5°/dB to -2°/dB at 9.5 GHz. At 9.0 GHz, the AM/PM conversion is $\pm$2°/dB and at 10 GHz the AM/PM conversion is negligible. When operated with pulsed gate voltages and pulsed rf, even lower AM/PM conversion is obtained.

Phase transients during pulsed rf-pulsed gate voltage operation were evaluated with the following test conditions: (1) gate and rf pulses turned on simultaneously; (2) 100 μsec pulse width for both gate and rf; (3) 50% duty cycle; and (4) the phase bridge balanced for a null at the turn-off edge of the rf pulse permitting intrapulse incremental phase shifts to be accurately measured. The drain current to the complete amplifier during the on-time is slightly less than 1 A. Because this must be provided within 20 nsec rise time of the amplifier, the drain supply circuitry must be able to tolerate a switching current transient of 50 A/μsec. It was found that the EMI filter type of feedthroughs typically used at bias circuit connection points are not suitable for pulsed applications because they resist rapid current changes and cause drain current ringing at a 400 kHz rate. When this ringing is removed from the measurements, the intrapulse phase shift is found to be under 5°.

Conclusions

The measured phase sensitivities and transients of FET power amplifiers with pulsed gate voltages are very low. FET amplifiers are thus suitable for phased array radar applications. These measurements indicate that the low level of phase sensitivities apparently inherent in the FET amplifiers will also result in low uncorrelated RMS phase shift due to external power supply, temperature, drive, and load pulling effects. Although pulsed gate operation results in simpler bias circuit requirements than pulsed drain operation, tighter restrictions are placed upon the FET. Besides providing good rf performance, tight controls on the device dc characteristics must be maintained. All devices must pinch off or the overall efficiency of the amplifier will be degraded. The drain-to-gate breakdown must be great enough to withstand the sum of the drain voltage, the gate voltage required for device pinchoff, and the maximum rf voltage swing. This can be as high as 15-20 volts. The devices selected in this program satisfied these breakdown requirements at the expense of power added efficiency.

In using a pulsed gate system, the drain supply circuitry must be designed to permit very rapid changes in drain current. Special attention must be given to the feedthrough filters to ensure that no distortion of the pulsed drain current occurs.

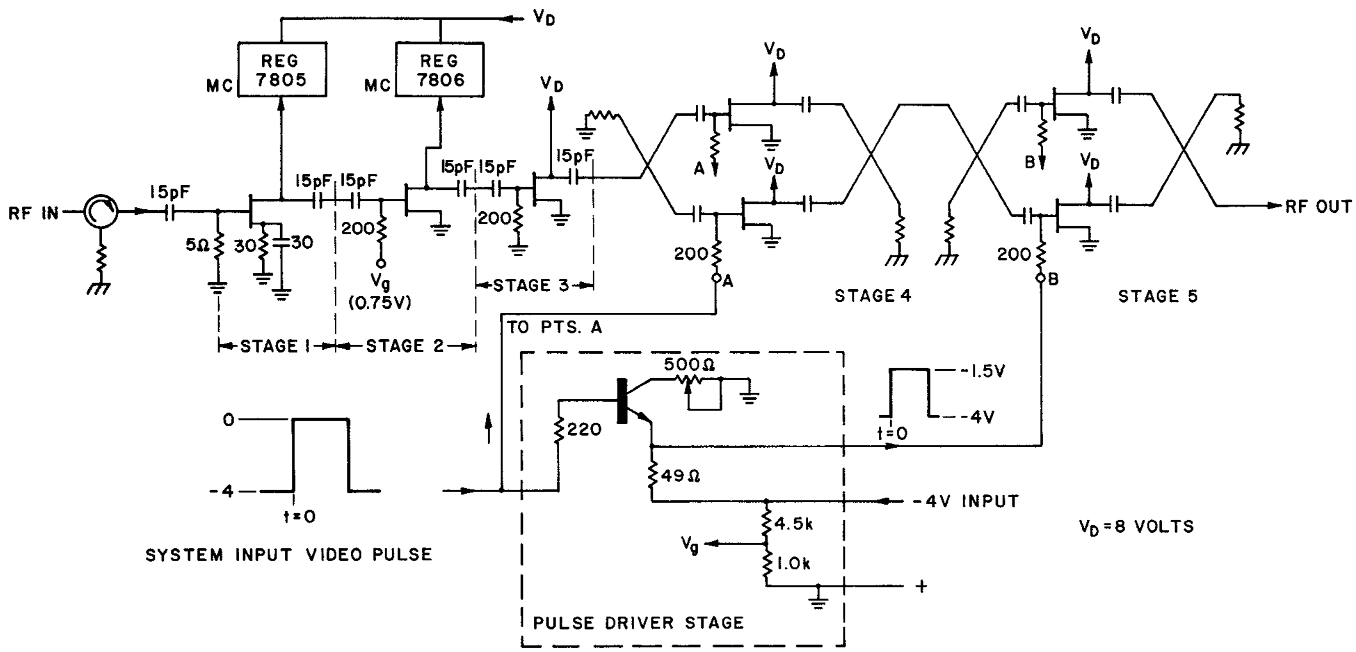


Figure 3. Composite schematic of overall FET amplifier bias (gate-drain potentials) and video pulse circuitry.

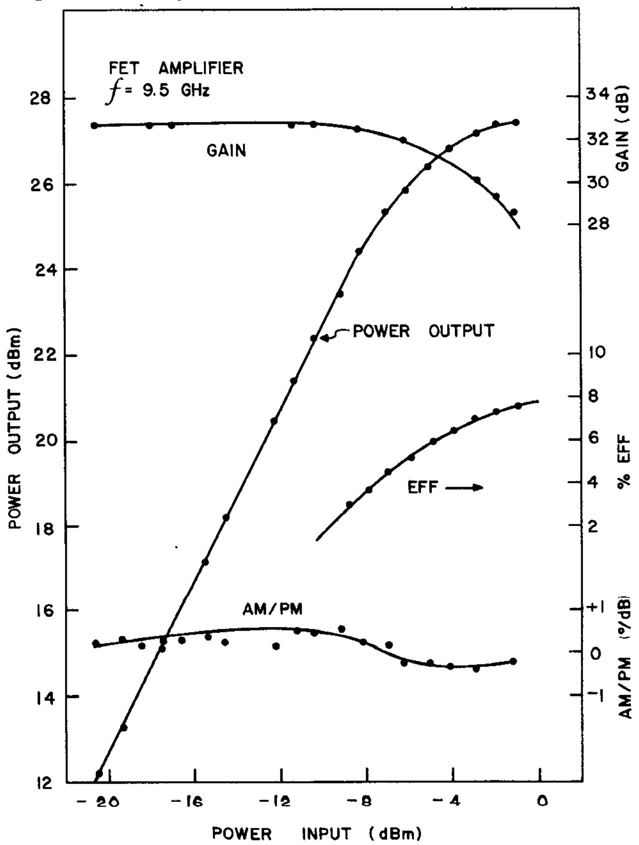


Figure 4. Output power, power added efficiency, gain, and AM/PM conversion vs. input power at 9.5 GHz (cw).

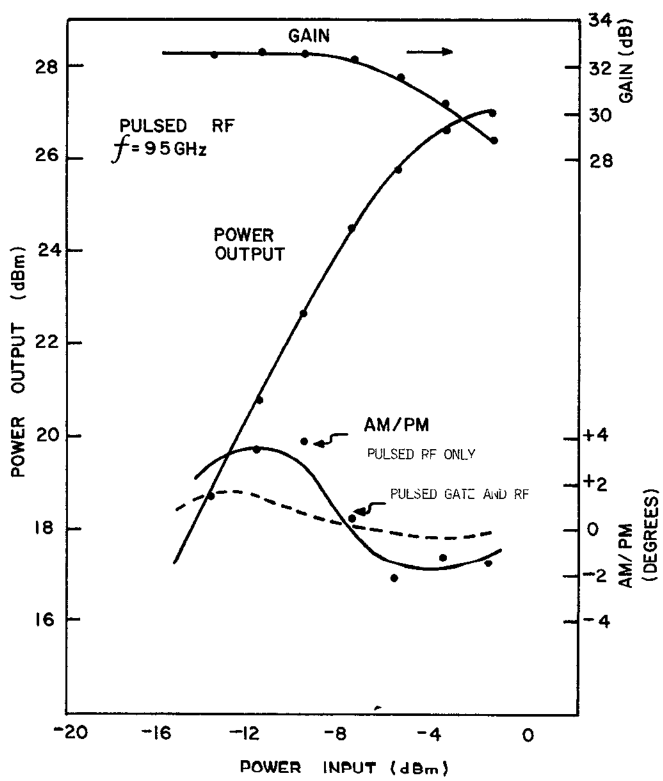


Figure 5. Midband (9.5 GHz) pulsed measurements.